CLAIMS

What is claimed is:

1. A method for selectively masking off undesirable states in selected scan cells, which cause test failures, from being compacted in selected pattern compactors for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an output-mask controller, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller including a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation;

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

2. The method of claim 1, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises generating a compressed stimulus, decompressing said compressed stimulus as said stimulus through said pattern generators, and shifting in said stimulus to all said scan cells in said selected scan-test mode during said shift-in operation; wherein said compressed stimulus is selectively generated internally or supplied externally from an ATE (automatic test equipment).

3. The method of claim 2, wherein each said pattern generator is selectively a broadcaster or a decompressor.

4. The method of claim 1, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises automatically generating said stimulus internally using said pattern generators in said selected self-test mode during said shift-in operation.

5. The method of claim 4, wherein each said pattern generator is selectively a pseudorandom pattern generator (PRPG) or a random pattern generator (RPG).

6. The method of claim 1, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using a load signal to preset said output-mask controller with a predetermined state for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during a selected shift-in operation.

7. The method of claim 1, wherein said shifting out said test response or said stimulus to said pattern compactors for compaction further comprises using said output-mask controller to generate a plurality of output-mask enable signals for controlling said output-mask network for selectively mask off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during said shift-out operation.

8. The method of claim 7, wherein said output-mask controller further comprises using an initialize signal to prevent said output-mask enable signals from masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during a selected shift-out operation.

9. The method of claim 7, wherein said output-mask controller further comprises a sequential output controller for generating a plurality of sequential-mask signals and said combinational output controller for generating said output-mask enable signals.

10. The method of claim 9, wherein said sequential output controller in said output-mask controller further comprises a plurality of selected cell-mask controllers for generating one or more selected cell-mask signals, a plurality of selected chain-mask controllers for generating one or more selected chain-mask signals, and a plurality of selected pattern-mask controllers for generating one or more selected pattern-mask signals; wherein said selected cell-mask signals, said selected chain-mask signals, and said selected pattern-mask signals are collectively referred to as said sequential-mask signals.

11. The method of claim 10, wherein each said cell-mask controller in said sequential output controller is a first finite-state machine generating one or more said selected cell-mask signals.

12. The method of claim 11, wherein said first finite-state machine is selectively a ring counter (RC) or a first range comparator.

13. The method of claim 10, wherein each said chain-mask controller in said sequential output controller is a second finite-state machine generating one or more said selected chain-mask signals.

14. The method of claim 13, wherein said second finite-state machine is selectively a first shift register (SR) or a range decoder.

15. The method of claim 10, wherein each said pattern-mask controller in said sequential output controller is a third finite-state machine generating one or more said selected pattern-mask signals.

16. The method of claim 15, wherein said third finite-state machine is selectively a second shift register (SR) or a second range comparator.

17. The method of claim 9, wherein said combinational output controller, comprising one or more said selected combinational logic networks other than said complete network of AND gates, further accepts said sequential-mask signals as inputs for generating said output-mask enable signals for controlling said output-mask network for selectively masking off all said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during said shift-out operation.

18. The method of claim 17, wherein each said selected combinational logic network further comprises one or more first selected combinational gates;

wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, Exclusive-OR (XOR) gate, Exclusive-NOR (XNOR) gate, multiplexor (MUX), or inverter (INV).

19. The method of claim 1, wherein said output-mask network further comprises one or more second selected combinational gates; wherein each said second selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

20. The method of claim 1, wherein each said pattern compactor is selectively a multi-input signature register (MISR) or a linear compactor; wherein said linear compactor further includes one or more third selected combinational gates; wherein each said third selected combinational gate is selectively an Exclusive-OR (XOR) gate or Exclusive-NOR (XNOR) gate..

21. An output-mask controller for generating a plurality of output-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an output-mask network, each scan chain comprising multiple scan cells coupled in series; said output-mask controller comprising:

(a) a sequential output controller for generating a plurality of sequential-mask signals; and

(b) a combinational output controller, comprising one or more selected combinational logic networks other than a complete network of AND gates, for generating a plurality of output-mask enable signals for controlling said output-mask network for selectively masking off

undesirable states in selected scan cells, which cause test failure, from being compacted in selected pattern compactors.

22. The output-mask controller of claim 21, further comprising using a load signal to preset said output-mask controller with a predetermined state for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

23. The output-mask controller of claim 21, further comprising using an initialize signal to prevent said output-mask enable signals from masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

24. The output-mask controller of claim 21, wherein said sequential output controller further comprises a plurality of selected cell-mask controllers for generating one or more selected cell-mask signals, a plurality of selected chain-mask controllers for generating one or more selected chain-mask signals, and a plurality of selected pattern-mask controllers for generating one or more selected pattern-mask signals; wherein said selected cell-mask signals, said selected chain-mask signals, and said selected pattern-mask signals are collectively referred to as said sequential-mask signals.

25. The output-mask controller of claim 24, wherein each said cell-mask controller in said sequential output controller is a first finite-state machine generating one or more said selected cell-mask signals.

26. The output-mask controller of claim 25, wherein said first finite-state machine is selectively a ring counter (RC) or a first range comparator.

27. The output-mask controller of claim 24, wherein each said chain-mask controller in said sequential output controller is a second finite-state machine generating one or more said selected chain-mask signals.

28. The output-mask controller of claim 27, wherein said second finite-state machine is selectively a first shift register (SR) or a range decoder.

29. The output-mask controller of claim 24, wherein each said pattern-mask controller in said sequential output controller is a third finite-state machine generating one or more said selected pattern-mask signals.

30. The output-mask controller of claim 29, wherein said third finite-state machine is second shift register (SR) or a second range comparator.

31. The output-mask controller of claim 21, wherein said combinational output controller, comprising one or more said selected combinational logic networks other than said complete network of AND gates, further accepts said sequential-mask signals as inputs for generating said output-mask enable signals for controlling said output-mask network for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

32. The output-mask controller of claim 31, wherein each said selected combinational logic network further comprises one or more first selected combinational gates; wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, Exclusive-OR (XOR) gate, Exclusive-NOR (XNOR) gate, multiplexor (MUX), or inverter (INV).

33. The output mask controller of claim 21, wherein said output-mask network further comprises one or more second selected combinational gates;

wherein each said second selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

34. A method for synthesizing an output-mask controller for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller comprising a sequential output controller and a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising the computer-implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or at gate-level that represents said scan-based integrated circuit into a design database;

(b) specifying input constraints on said output-mask controller;

(c) synthesizing said output-mask controller on said design database according to said input constraints; and

(d) generating synthesized HDL code for said output-mask controller in a selected RTL or gate-level format.

35. The method of claim 34, wherein said specifying input constraints on said output-mask controller further comprises automatically generating said input constraints based on said design database.

36. The method of claim 34, wherein said synthesizing said output-mask controller on said design database according to said input constraints further comprises synthesizing said sequential output controller for generating a plurality of sequential-mask signals, and synthesizing said combinational output controller for generating a plurality of output-mask enable signals for controlling said output-mask network for selectively masking off undesirable states in selected scan cells, which cause test failure, from being compacted in selected pattern compactors.

37. The method of claim 36, wherein said synthesizing said output-mask controller further comprises using a load signal to preset said output-mask controller with a predetermined state for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

38. The method of claim 36, wherein said synthesizing said output-mask controller further comprises using an initialize signal to prevent said output-mask enable signals from masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

39. The method of claim 36, wherein said sequential output controller in said output-mask controller further comprises a plurality of selected cell-mask controllers for generating one or more selected cell-mask signals, a plurality of selected chain-mask controllers for generating one or more selected chain-mask signals, and a plurality of selected pattern-mask controllers for generating one or more selected pattern-mask signals; wherein said selected cell-mask signals, said selected chain-mask signals, and said selected pattern-mask signals are collectively referred to as said sequential-mask signals.

40. The method of claim 39, wherein each said cell-mask controller in said sequential output controller is a first finite-state machine generating one or more said selected cell-mask signals.

41. The method of claim 40, wherein said first finite-state machine is selectively a ring counter (RC) or a first range comparator.

42. The method of claim 39, wherein each said chain-mask controller in said sequential output controller is a second finite-state machine generating one or more said selected chain-mask signals.

43. The method of claim 42, wherein said second finite-state machine is selectively a first shift register (SR) or a range decoder.

44. The method of claim 39, wherein each said pattern-mask controller in said sequential output controller is a third finite-state machine generating one or more said selected pattern-mask signals.

45. The method of claim 44, wherein said third finite-state machine is selectively a second shift register (SR) or a second range comparator.

46. The method of claim 36, wherein said combinational output controller, comprising one or more said selected combinational logic networks other than said complete network of AND gates, further accepts said sequential-mask signals as inputs for generating said output-mask enable signals for controlling said output-mask network for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

47. The method of claim 46, wherein each said selected combinational logic network further comprises one or more first selected combinational gates;

wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, Exclusive-OR (XOR) gate, Exclusive-NOR (XNOR) gate, multiplexor (MUX), or inverter (INV).

48. The method of claim 36, wherein said synthesizing said output-mask controller on said design database according to said input constraints further comprises synthesizing said output-mask network using said output-mask enable signals for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors.

49. The method of claim 48, wherein said output-mask network further comprises one or more second selected combinational gates; wherein each said second selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

50. A method for selectively driving selected constant logic values into all scan cells in selected scan chains for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an input chain-mask controller, and an input-mask network, each scan chain comprising multiple scan cells coupled in series, the input chain-mask controller connected to the input-mask network; said method comprising:

   (a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit by selectively forcing said selected constant logic values into all said scan cells in said selected scan chains during a shift-in operation;

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction, while shifting in a new stimulus to all said scan cells in said scan-based integrated circuit, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

51. The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises generating a compressed stimulus, decompressing said compressed stimulus as said stimulus through said pattern generators, and shifting in said stimulus to all said scan cells in said selected scan-test mode during said shift-in operation; wherein said compressed stimulus is selectively generated internally or supplied externally from an ATE (automatic test equipment).

52. The method of claim 51, wherein each said pattern generator is selectively a broadcaster or a decompressor.

53. The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises automatically generating said stimulus internally using said pattern generators in said selected self-test mode during said shift-in operation.

54. The method of claim 53, wherein each said pattern generator is selectively a pseudorandom pattern generator (PRPG) or a random pattern generator (RPG).

55. The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using a load signal to preset said input chain-mask controller with a predetermined state to selectively force said selected constant logic values into all said scan cells in said selected scan chains during a selected shift-in operation.

56. The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using said input chain-mask controller to generate a plurality of input-mask enable signals for controlling said input-mask network to selectively force said selected constant logic values into all said scan cells in said selected scan chains during said shift-in operation.

57. The method of claim 56, wherein said input chain-mask controller further comprises using an initialize signal to prevent said input-mask enable signals from forcing said selected constant logic values into all said scan cells in said selected scan chains.

58. The method of claim 56, wherein said input chain-mask controller is a finite-state machine generating said input-mask enable signals.

59. The method of claim 58, wherein said finite-state machine is selectively a shift register (SR) or a range decoder.

60. The method of claim 50, wherein said input-mask network further comprises one or more first selected combinational gates; wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

61. The method of claim 50, wherein each said pattern compactor is selectively a multi-input signature register (MISR) or a linear compactor; wherein said linear compactor further includes one or more second selected combinational gates; wherein each said second selected combinational gate is selectively an Exclusive-OR (XOR) gate or Exclusive-NOR (XNOR) gate.

62. An input chain-mask controller for generating a plurality of input-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an input-mask network, each scan chain comprising multiple scan cells coupled in series; said input chain-mask controller comprising:

a finite-state machine for generating said input-mask enable signals for controlling said input-mask network to selectively force selected constant logic values into all scan cells in selected scan chains.

63. The input chain-mask controller of claim 62, wherein said finite-state machine further comprises using a load signal to preset said input chain-mask controller with a predetermined state to selectively force said selected constant logic values into all said scan cells in said selected scan chains.

64. The input chain-mask controller of claim 62, wherein said finite-state machine further comprises using an initialize signal to prevent said input-mask enable signals from forcing said selected constant logic values into all said scan cells in said selected scan chains.

65. The input chain-mask controller of claim 62, wherein said finite-state machine is selectively a shift register (SR) or a range decoder.

66. The input chain-mask controller of claim 62, wherein said input-mask network further comprises one or more selected combinational gates; wherein each said selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

67. A method for synthesizing an input chain-mask controller for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an input-mask network, each scan chain comprising multiple scan cells coupled in series; said method comprising the computer-implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or at gate-level that represents said scan-based integrated circuit into a design database;

(b) specifying input constraints on said input chain-mask controller;

(c) synthesizing said input chain-mask controller on said design database according to said input constraints; and

(d) generating synthesized HDL code for said input chain-mask controller in a selected RTL or gate-level format.

68. The method of claim 67, wherein said specifying input constraints on said input chain-mask controller further comprises automatically generating said input constraints based on said design database.

69. The method of claim 67, wherein said synthesizing said input chain-mask controller on said design database according to said input constraints further comprises synthesizing said finite-state machine for generating a plurality of input-mask enable signals for controlling said input-mask network to selectively force selected constant logic values into all scan cells in selected scan chains.

70. The method of claim 69, wherein said synthesizing said input chain-mask controller on said design database according to said input constraints further comprises using a load signal to preset said input chain-mask controller with a predetermined state to selectively force said selected constant logic values into all said scan cells in said selected scan chains.

71. The method of claim 69, wherein said synthesizing said input chain-mask controller on said design database according to said input constraints further comprises using an initialize signal to prevent said input-mask enable signals from forcing said selected constant logic values into all said scan cells in said selected scan chains.

72. The method of claim 69, wherein said finite-state machine is selectively a shift register (SR) or a range decoder.

73. The method of claim 69, wherein said synthesizing said input chain-mask controller on said design database according to said input constraints further comprises synthesizing said input-mask network using said input-mask enable signals to selectively force said selected constant logic values into all said scan cells in said selected scan chains.

74. The method of claim 73, wherein said input-mask network further comprises one or more selected combinational gates; wherein each said

selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, or multiplexor (MUX).

75. A method for generating stimuli and test responses for testing faults in a scan-based integrated circuit in a selected scan-test mode or a selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, a selected output-mask controller, a selected output-mask network, a selected input chain-mask controller, and a selected input-mask network, each scan chain comprising multiple scan cells coupled in series, the selected output-mask controller including a sequential output controller and a combinational output controller connected to the selected output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a network of AND gates, the selected input chain-mask controller connected to the selected input-mask network; said method comprising the computer implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or at gate-level that represents said scan-based integrated circuit into a sequential circuit model;

(b) specifying input constraints on said scan-based integrated circuit during a shift-in, a capture, or a shift-out operation, the input constraints including a predetermined state of said selected output-mask controller and said selected input chain-mask controller;

(c) transforming said sequential circuit model into an equivalent combinational circuit model; and

(d) generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints.

76. The method of claim 75, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing fault simulation on said equivalent combinational circuit model selectively using a selected set of predetermined patterns as said stimuli and said test responses in said selected scan-test mode, or a selected set of pseudorandom patterns as said stimuli and said test responses in said selected self-test mode.

77. The method of claim 75, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing combinational ATPG (automatic test pattern generation) on said equivalent combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

78. The method of claim 75, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

79. The method of claim 75, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.

80. A computer-readable memory having computer-readable program code embodied therein for causing a computer system to perform a method for generating stimuli and test responses for testing faults in a scan-based integrated circuit in a selected scan-test mode or a selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, a selected output-mask controller, a selected output-mask network, a selected input chain-mask controller, and a selected input-mask network, each scan chain comprising multiple scan cells coupled in series, the selected output-mask controller including a sequential output controller and a combinational output controller connected to the selected output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a network of AND gates, the selected input chain-mask controller connected to the selected input-mask network; said method comprising the computer implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or at gate-level that represents said scan-based integrated circuit into a sequential circuit model;

(b) specifying input constraints on said scan-based integrated circuit during a shift-in, a capture, or a shift-out operation, the input constraints including a predetermined state of said selected output-mask controller and said selected input chain-mask controller;

(c) transforming said sequential circuit model into an equivalent combinational circuit model; and

(d) generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints.

81. The computer-readable memory of claim 80, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing fault simulation on said equivalent combinational circuit model selectively using a selected set of predetermined patterns as said stimuli and said test responses in said selected scan-test mode, or a selected set of pseudo-random patterns as said stimuli and said test responses in said selected self-test mode.

82. The computer-readable memory of claim 80, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing combinational ATPG (automatic test pattern generation) on said equivalent combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

83. The computer-readable memory of claim 80, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

84. The computer-readable memory of claim 80, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.

85. An electronic design automation system comprising: a processor; a bus coupled to said processor; and a computer-readable memory coupled to said bus and having computer-readable program code embodied therein for causing said electronic design automation system to perform a method for generating stimuli and test responses for testing faults in a scan-based integrated circuit in a selected scan-test mode or a selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, a selected output-mask controller, a selected output-mask network, a selected input chain-mask controller, and a selected input-mask network, each scan chain comprising multiple scan cells coupled in series, the selected output-mask controller including a sequential output controller and a combinational output controller connected to the selected output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a network of AND gates, the selected input chain-mask controller connected to the selected input-mask network; said method comprising the computer implemented steps of:

(a) compiling the HDL (hardware description language) code modeled at RTL (register-transfer level) or at gate-level that represents said scan-based integrated circuit into a sequential circuit model;

(b) specifying input constraints on said scan-based integrated circuit during a shift-in, a capture, or a shift-out operation, the input constraints including a predetermined state of said selected output-mask controller and said selected input chain-mask controller;

(c) transforming said sequential circuit model into an equivalent combinational circuit model; and

(d) generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints.

86. The system of claim 85, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing fault simulation on said equivalent combinational circuit model selectively using a selected set of predetermined patterns as said stimuli and said test responses in said selected scan-test mode, or a selected set of pseudorandom patterns as said stimuli and said test responses in said selected self-test mode.

87. The system of claim 85, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises performing combinational ATPG (automatic test pattern generation) on said equivalent combinational circuit model to generate said stimuli and said test responses in said selected scan-test mode.

88. The system of claim 85, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating HDL test benches according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit using simulation methods.

89. The system of claim 85, wherein said generating said stimuli and said test responses on said equivalent combinational circuit model according to said input constraints further comprises generating ATE (automatic test equipment) test programs according to said stimuli and said test responses for verifying the correctness of said scan-based integrated circuit in said ATE.